CLAIMS

1. A method for combining a plurality of read miss requests into a single network packet for a network of a plurality of processors comprising:

generating an entry in a Miss Address File (MAF) for each of the plurality of read miss requests;

delaying the MAF controller from forwarding the plurality of read miss requests for a predetermined number of cycles; and

combining the plurality of read miss requests that are destined to the same processor into a single network packet; and

forwarding the single network packet to that same processor.

2. The method of claim 1 wherein the plurality of read miss requests that are destined to the same processor occur in a burst from either a program stream through an array in a scientific application or through leaf nodes of B+ trees in a database program.

3. The method of claim 1 wherein the network is a cache-coherent shared memory configuration.

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4. A method for combining a plurality of read miss requests into a single network packet for a network of a plurality of processors comprising:

generating an entry in a Miss Address File (MAF) for each of the plurality of read miss

10   requests;

delaying the MAF controller from forwarding the plurality of read miss requests for a predetermined number of cycles; and

combining the plurality of read miss requests that are destined to the same processor and that occur in bursts into a single network packet; and

15   forwarding the single network packet to that same processor.

5. The method of claim 4 wherein the plurality of read miss requests that occur in bursts come from either a program stream through an array in a scientific application or through leaf nodes of B+ trees in a database program.

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6. The method of claim 4 wherein the network is a cache-coherent shared memory configuration.

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5   7. A method for combining a plurality of exclusive access requests into a single network

packet for a network of a plurality of processors comprising:

identifying a plurality of exclusive access requests by at least one of the plurality

of processors for writing a cache block to a local cache; and

combining the plurality of exclusive access requests into a single network packet

10   to be transmitted in the network.

8. The method of claim 7 wherein the plurality of exclusive access requests is granted by a

home node in the network.

15   9. A system comprising:

a plurality of processors, coupled to a network and memory, with each processor having a

merge buffer to:

write data into an entry in the merge buffer upon retiring a store operation and

deallocate an entry in the merge buffer, and to identify a plurality of entries in the

20   merge buffer that are mapped to the same processor among the plurality of processors and

to combine the plurality of entries in the merge buffer that are mapped to the same

processor among the plurality of processors into a single network packet.

10. The system of claim 9 wherein the network is a point to point link among a plurality

of cache agents and home agents.

25   11. The system of claim 9 wherein the system is a cache-coherent shared-memory

multiprocessor system.